CSC 242 Computer Architecture and Organization Spring 2021

# Homework 3: Computer Architecture and Organization (CSC 242)

**Due: Friday, April 23, 11:59 pm**

**NOTE:** Please type your answers to the following questions and submit a pdf or doc on the MOODLE.

**1. Memory Addressing**

1. **[5 points]** For a byte-addressable memory, how much memory can be accessed using a 64 bit address? Express your answer using metric prefixes (kilo, mega, giga, etc.).

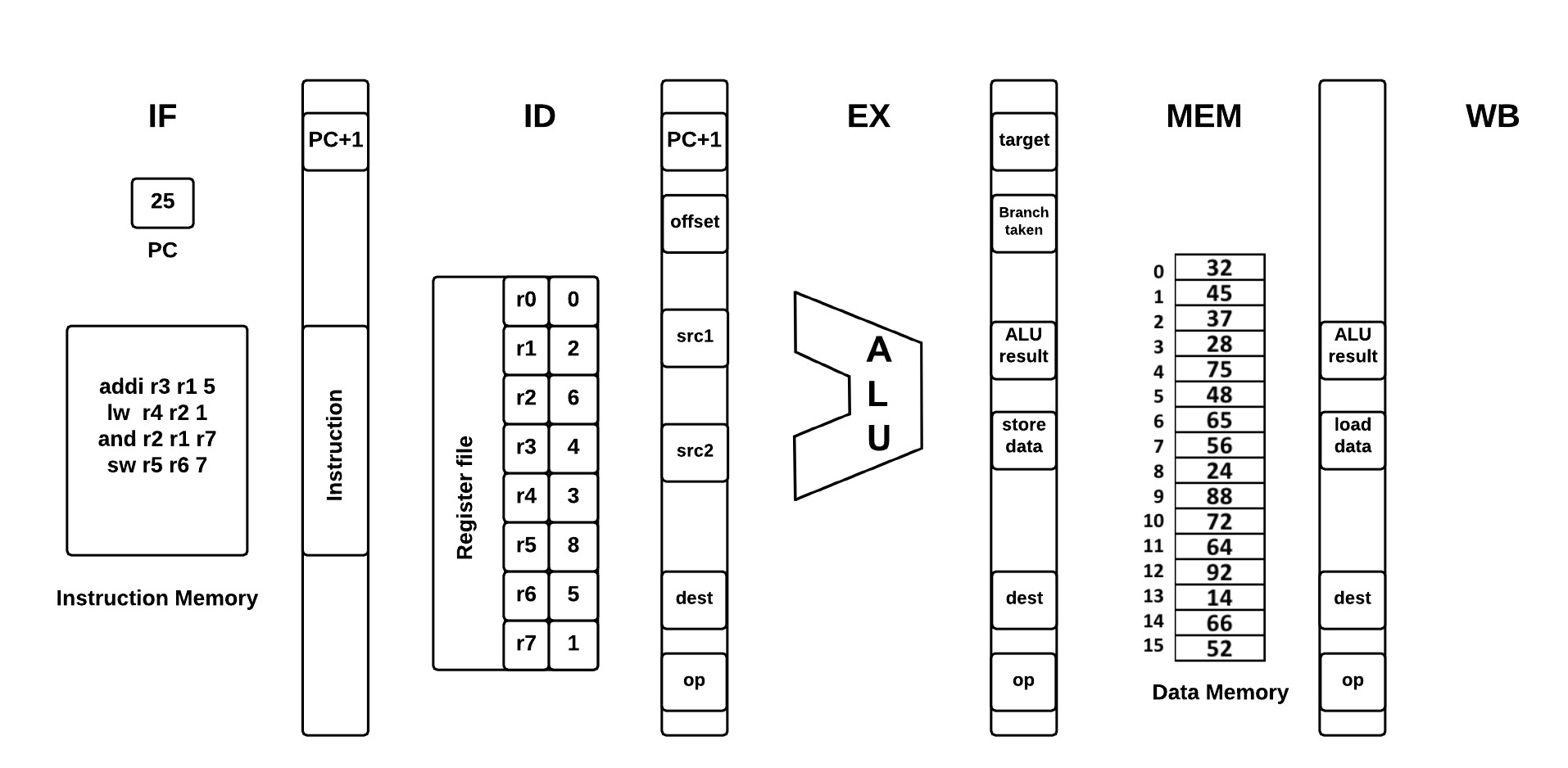
264 bytes = 28 \* 250 bytes = 14TB

1. **[5 points]** For a byte-addressable memory, how many address bits are needed for 128 GB memory?

Log2 128GB = log2 (27 \* 230) = log2(237) = 37 bits

1. **[5 points]** For a word-addressable memory, how much memory can be accessed using a 32 bit address? (Assume that a word is 32 bits.)
2. 232 cells \* 4bytes/cell = 232 \* 22 bytes = 16GB
3. **[5 points]** For a word-addressable memory, how many address bits are needed for 512 GB memory? (Also, assume that a word is 32 bits.)
4. Log2 512GB/4bytes = log2(29 \* 2-2) bytes = log2(27) = 128 bits

**2. [10+5 points]** Assume that we have the following instruction sequence in the instruction memory with the given value of the Program Counter (PC=25) on a pipelined MIPS processor.



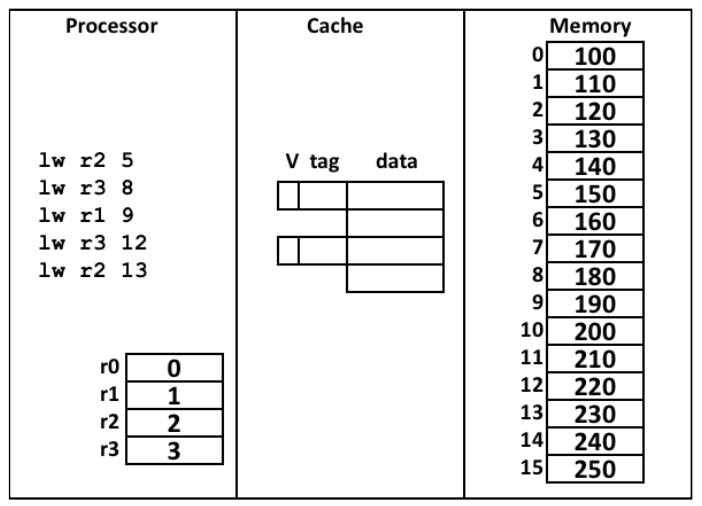
1. Create an execution time graph for the above instruction sequence for its pipelined implementation without stalls. (10 points)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Time/Cycle: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| addi r3 r1 5 | IF | ID | EX | ME | WB |  |  |  |
| lw r4 r2 1 |  | IF | ID | EX | ME | WB |  |  |
| and r2 r1 r7 |  |  | IF | ID | EX | ME | WB |  |
| sw r5 r6 7 |  |  |  | IF | ID | EX | ME | WB |

1. What is the average number of cycles per instruction (CPI) for this implementation? (5 points)
2. 8 cycles / 4 instructions = 2 cycles per instruction

**3. [10+5 points]** (a) Assume we have a system consisting of 4 registers named r0–r3 inside the processor, a cache with 2 cache blocks which are initially empty, and 16 word-addressable memory indexed by 4 bit addresses, determine how many cache hits and misses would occur in the system for the following sequence of instructions inside the processor. (10 points)

There are 3 cache misses, and 2 cache hits.



(b) Consider a word-addressable memory system has 32-bit addresses and a cache block stores 32 words. How many bits comprise the tag and block offset in a cache address? (5 points)

Tag = 27 Block Offset = 5

**4. [5+15+5 points]** (a) For the following sequence of MIPS assembly language instructions, calculate the number of data hazards would occur during their executions without stalls in a pipelined implementation. (5 points) 4 hazards encountered R3, R3, R6, R6

add r3 r4 r2

sub r5 r3 r1

lw r6 r3 0x45

or r7 r3 r6

sw r6 r5 0x12

Generate an execution time graph to avoid data hazards in the same pipelined implementation.(15 points)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Time/Cycle | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| add r3 r4 r2 | IF | ID | EX | ME | WB |  |  |  |  |  |  |  |  |  |
| sub r5 r3 r1 |  | IF | ID | ID | ID | EX | ME | WB |  |  |  |  |  |  |
| lw r6 r3 0x45 |  |  | IF | IF | IF | ID | EX | ME | WB |  |  |  |  |  |
| or r7 r3 r6 |  |  |  |  |  | IF | ID | ID | ID | EX | ME | WB |  |  |
| sw r6 r5 0x12 |  |  |  |  |  |  | IF | IF | IF | ID | EX | ME | WB |  |

1. What is the CPI value for executing these instructions with stalls in their pipelined implementation? (5 points)
2. CPI = 13 cycles / 5 instructions = 2.6 cycles per instruction
3. **[15 points]** Given a computer with L1, L2, and L3 caches. Of all the memory references, 60% hit on L1 cache, 30% hit on L2 cache, 10% miss on L3 cache. Following are the access times:

L1 cache access time: 5 ns

L2 cache access time: 15 ns

L3 cache access time: 25 ns

Main memory access time: 60 ns

Considering L2 cache access will start only if there is a miss in L1 cache, L3 cache access will start only if there is a miss in L2 cache, similarly, main memory access will start only after L1, L2, and L3 cache misses, compute the average memory access time for this system.

.6 \* 5 + .4(.3 \* 15 + .7(.1 \* 25 + .9 \* 60)) = 20.62 ns

1. **[10 points]** Consider an application A running on a single cycle datapath system comprising of data and instruction caches coupled with main memory. Assume that 80% of the instruction fetches hit in the instruction cache, 70% of the memory references hit in the data cache and 40% of the operations access data memory. On cache misses, the system takes 20 cycles to access main memory. The processor is stalled for that entire time.

What is the CPI value for the application A to run on this system?

.7 \* .8 + .3 \* 20 = 6.56

.6 \* .8 + .4 \* 6.56 = 5.77